Lab 10

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Prelab:

Diagram, schematic

Description automatically generated

Purpose:

The purpose of lab 10 was to design a 4-bit up counter circuit in Xilinx Vivado with VHDL.

Lab Procedure:

We started the lab by opening Vivado and creating an RTL project that was set to ‘VHDL’ target language. We continued by creating a design source file called UpCounter with I/O ports for the file. The I/Os were clk, SevenSeg, reset, counter, and Anode\_to\_activate. We then wrote code to simulate the up counter and to correctly display numbers on the seven-segment display.

We then ran the Behavioral Simulation and took note of the waveform output, created one final program called UpCounterTest to display the up counter, then ran Synthesis, Implementation, and finally Generated Bitstream. We then connected the Basys 3 board to the computer and watched the up-counter work.

Vivado Code-

Graphical user interface, text, application

Description automatically generated

Graphical user interface

Description automatically generated with low confidence

Basys 3 Board-

A picture containing text, electronics, circuit

Description automatically generated

A picture containing text, electronics

Description automatically generatedA picture containing text, electronics, circuit

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Conclusion:

In this lab, we made a 4-bit up counter in Xilinx Vivado with VHDL. The results of this lab produced a functional up counter that counted up from 0000 to 1111 automatically and automatically reset to 0000 when it passed 1111.

Finally, I believe physically constructing a circuit is more beneficial to my learning.

Observations:

The main observation I have to improve my performance on future experiments is to become more familiar with the code for an up counter.